

CIR-W5SUSE5608G

DDR5 WIDE TEMP. SO-DIMM 5600MHz 8GB

Description

CIR-W5SUSE5608G is a 1G x 64-bit (8GB) DDR5-5600 CL46 SDRAM (Synchronous DRAM), 1Rx16, memory module, based on eight 1G x 16-bit FBGA components. The SPD is programmed to JEDEC standard latency DDR5-5600 timing of 46-45-45 at 1.1V. Each 262-pin SO-DIMM uses gold contact fingers. Power management integrated circuit (PMIC) provides better signal integrity and more stable power. Original DRAM chips and all components are stringently tested for the highest level of compatibility, reliability, and performance.

Specifications

| | |
|------------------------|-------------------|
| Density | 8GB |
| Pin Count | 262pin |
| Type | Unbuffered |
| Dimensions | 69.60mm x 30.00mm |
| ECC | Non-ECC |
| Component Config | 1G x 16 bit |
| Data Rate | 5600 MHz |
| CAS Latency | 46 |
| Voltage | 1.1V |
| PCB Layers | 10 |
| Operating Temp.(TCASE) | -40°C~+85°C |
| Module Ranks | Single Rank |

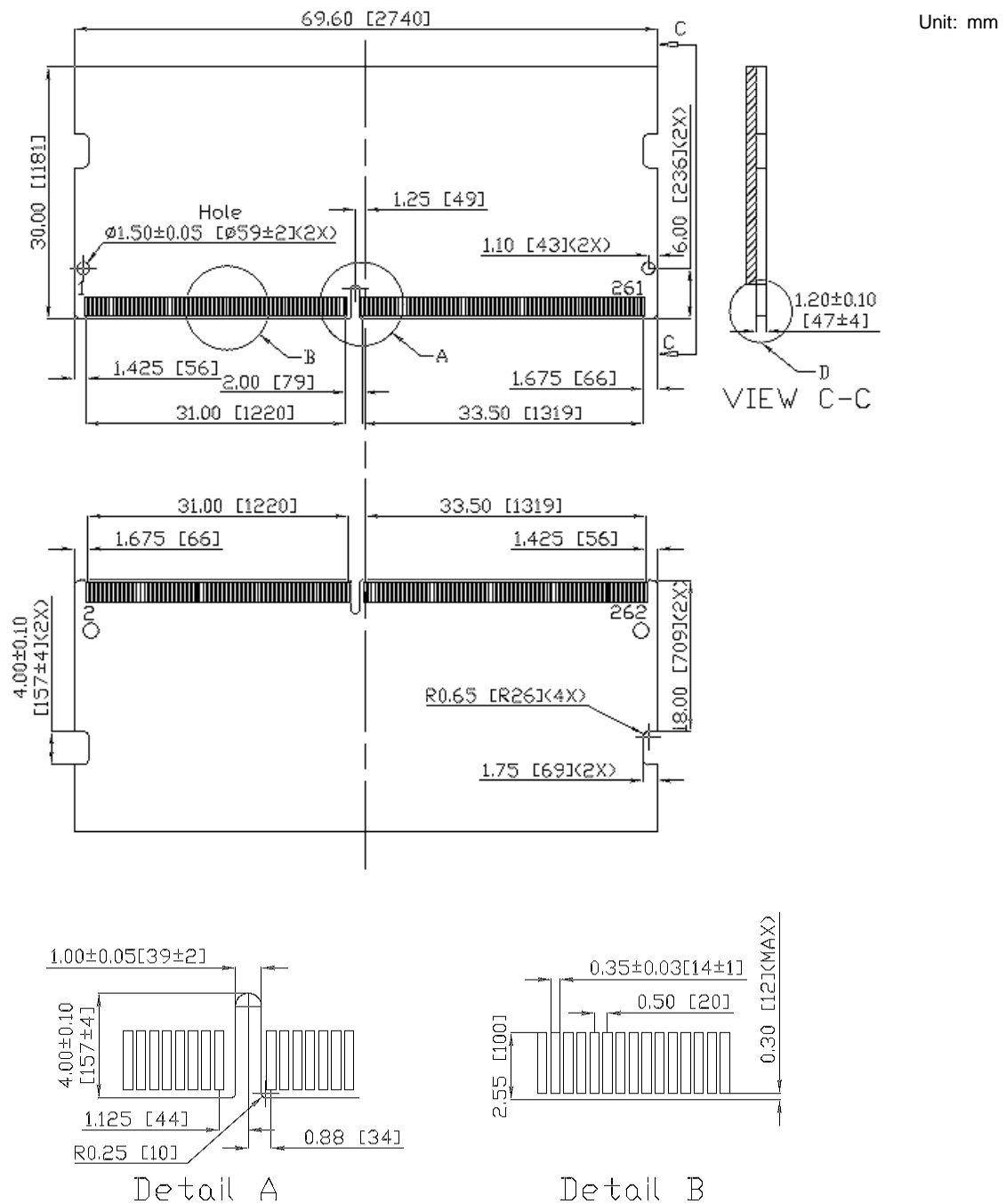
Features

- JEDEC Standard 262-pin Small Outline Dual In-Line Memory Module
- VDD = VDDQ = 1.1V (1.067V~1.166V)
- VPP = VDDSPD =1.8V
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42,46,50
- PMIC on DIMM, nominal supply 5V, VIN_Bulk input supply range: 4.25 V to 5.5 V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- On-Die ECC
- SPD Hub with Thermal Sensor
- Fly-By topology
- Terminated control, command and address bus
- RoHS Compliant and Halogen free

Speed Grade

| Frequency Grade | Data Transfer Rate | CAS Latency Support | | | CL-tRCD-tRP |
|-----------------|--------------------|---------------------|-----|------|-------------|
| | | CL40 | TBC | CL46 | |
| DDR5-5600 | PC5-44800 | 4800 | TBC | 5600 | 46-45-45 |

Package Dimensions



Tolerances: ± 0.15 mm unless otherwise specified