CIR-S2DUMG8001G

DDR2 DIMM 800MHz 1GB

Description

The CIR-S2DUMG8001G is 128M wordsx64 bits, 1 rank DDRII SDRAM unbuffered module, mounting 8 pieces of 1G bits DDR2 SDRAM sealed in FBGA (µBGA®) package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 4bits prefetch pipelined architecture. Data strobe (DQS and /DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each FBGA (µBGA) on the module board.

Specifications

Density	1GB
Pin Count	240pin
Type	Unbuffered
Dimensions	133.35mm x 30.00mm
ECC	Non-ECC
Component Config	128M x 8 bit
Data Rate	800 MHz
CAS Latency	6
Voltage	1.8V
PCB Layers	6
Operating Temp.(TCASE)	0°C~+85°C
Module Ranks	Single Rank

Features

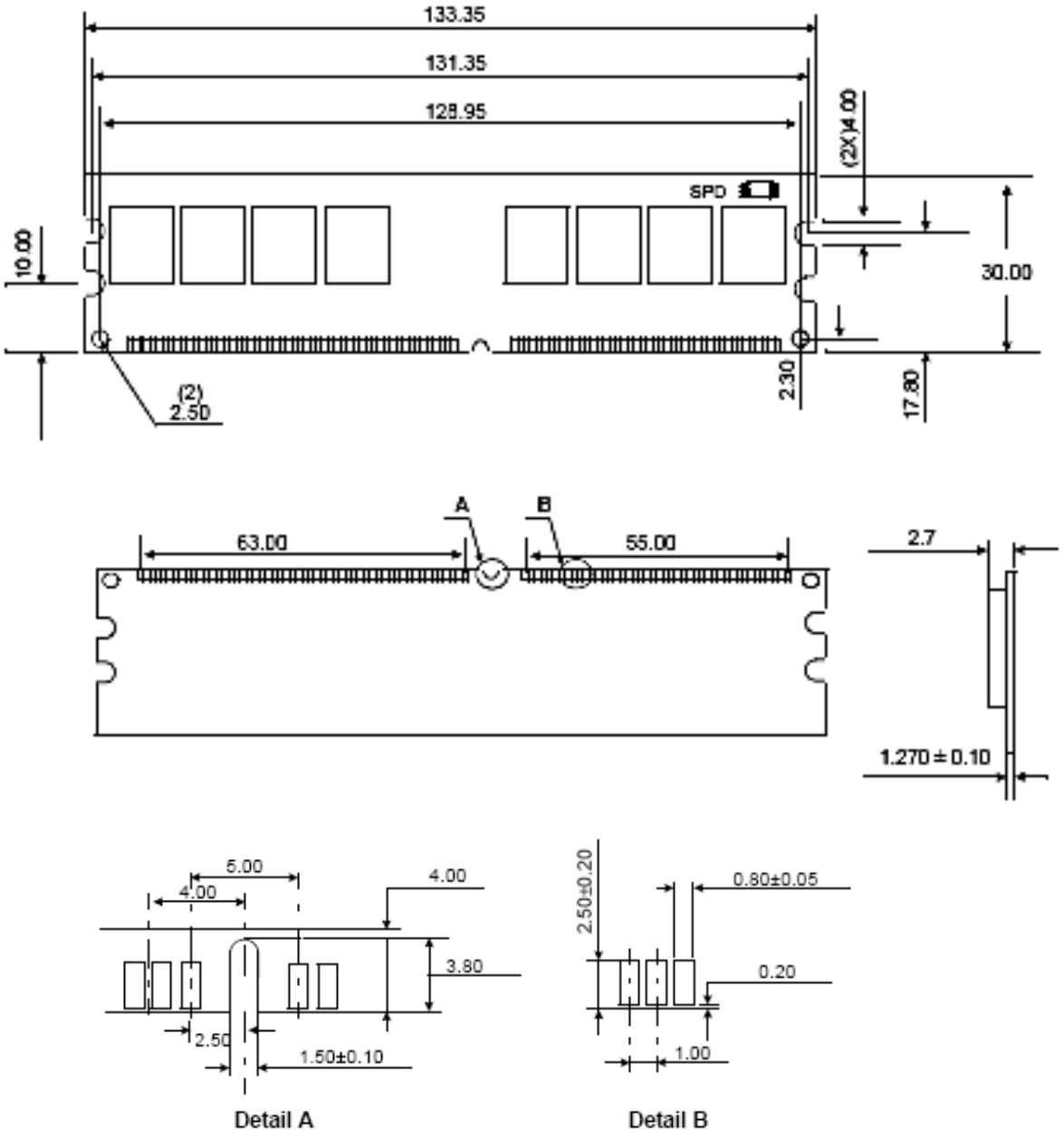
- Lead-Free products are ROHS compliant
- 240-pin Dual in-line memory module(DIMM)
- JEDEC standard 1.8V I/O(SSTL_18-compatible)
- 8 Banks
- Burst Length：4,8
- CAS Latency (CL)：4,5,6
- 4-bit prefetch pipelined architecture
- Auto refresh and self refresh supported
- Differential clock inputs (CK & /CK)
- DLL align DQ and DQS transitions with CK transitions
- DQS can be disabled for single-ended Data Strobe operation
- Bi-directional differential Data-Strobe (DQS &/DQS) is transmitted/received with data for capturing data at the receiver
- Posted CAS
- Data mask(DM) for write data
- ODT (On-Die Termination)
- OCD (Off-Chip Driver Impedance Adjustment)
- 8192 refresh cycle /64ms
- Serial presence detect with EEPROM
- Gold edge contacts
- Average Refresh Period
  7.8us at 0°C ≦ TCASE ≦ +85°C
  3.9us at＋ 85℃ ＜TCASE≦＋95℃

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support			CL-tRCD-tRP
		CL4	CL5	CL6	
DDR2-800	PC2-6400	533	667	800	6-6-6

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified