CIR-S1DUME4001G

DDR1 DIMM 400MHz 1GB

Description

The CIR-S1DUME4001G is 128M words X 64 bits, 2 ranks Double Data Rate (DDR) SDRAM unbuffered modules, mounting 16 pieces of 512GB bit DDR SDRAM (64Mx8) sealed in TSOPII package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DDL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each TSOPII on the module board.

Specifications

Density	1GB
Pin Count	184pin
Type	Unbuffered
Dimensions	133.35mm x 29.464mm
ECC	Non-ECC
Component Config	64M x 8 bit
Data Rate	400 MHz
CAS Latency	3
Voltage	2.6V
PCB Layers	6
Operating Temp.(TCASE)	0°C~+70°C
Module Ranks	Dual Rank

Features

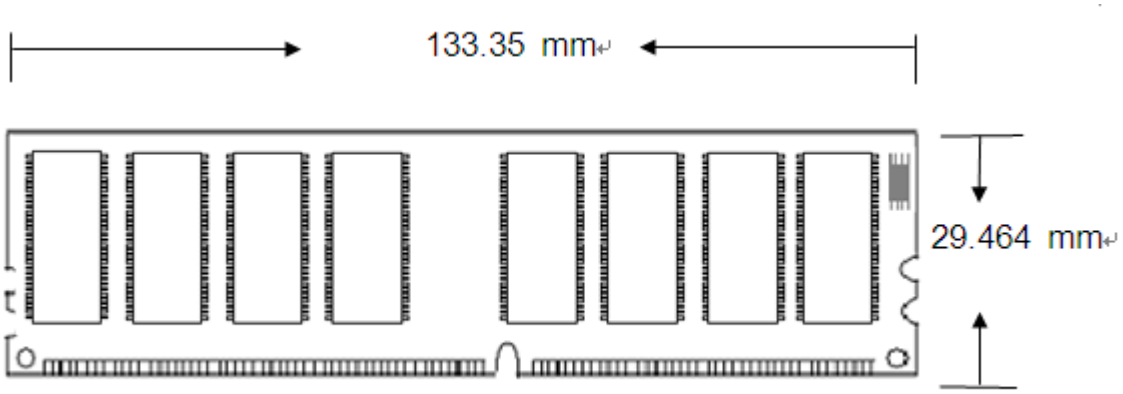
- Power supply : VDD: 2.6V ± 0.1V, VDDQ: 2.6V ± 0.1V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe[DQ](x4,x8)& [L(U)DQS] (x16)
- Differential clock inputs(CK and /CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency : 2.5 / 3
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect with EEPROM
- SSTL_2 Interface
- 66pin TSOP
- All of Lead-Free products are compliant for RoHS

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support		CL-tRCD-tRP
		CL2.5	CL3	
DDR-400	PC-3200	266	333/400	3-3-3

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified