CIR-S3DVSIM1002G

DDR3 VLP-DIMM 1066MHz 2GB

Description

The CIR-S3DVSIM1002G is 256M words X 64 bits, 1 rank. Unbuffered Dual In-Line Memory Module (DIMM). DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 240pin glass-epoxy substrate. Provide a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

Specifications

Density	2GB
Pin Count	240pin
Type	Unbuffered
Dimensions	133.35mm x 18.30mm
ECC	Non-ECC
Component Config	256M x 8 bit
Data Rate	1066 MHz
CAS Latency	7
Voltage	1.5V
PCB Layers	8
Operating Temp.(TCASE)	0°C~+85°C
Module Ranks	Single Rank

Features

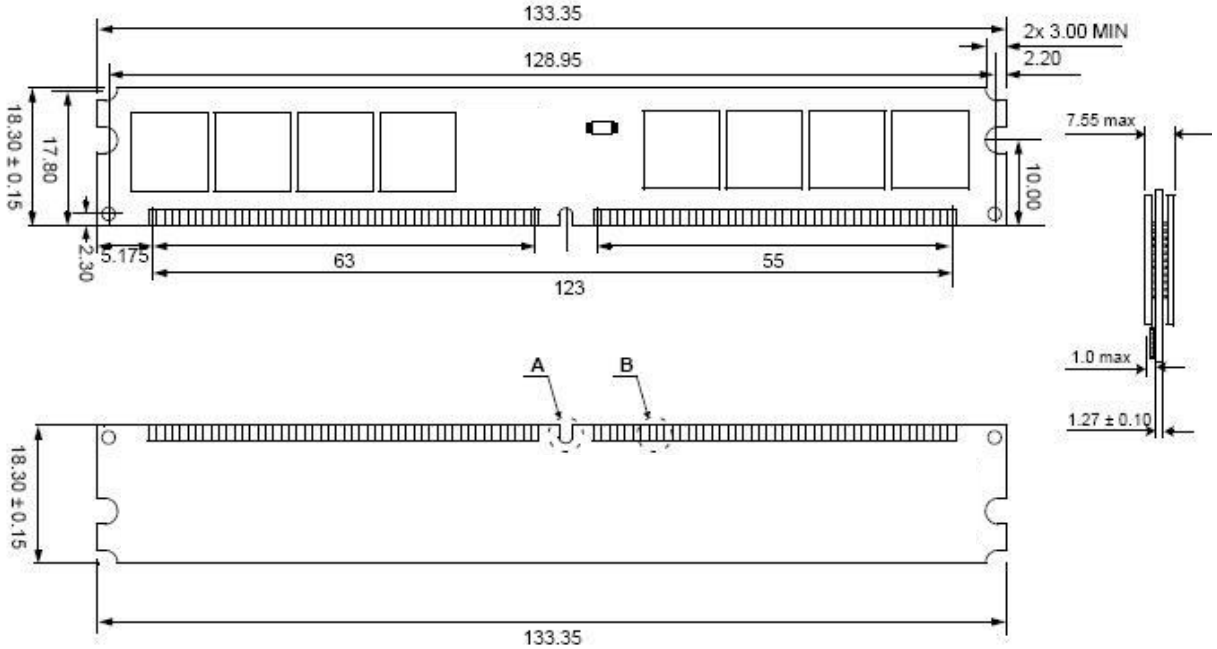
- Data rate: 1066MHz
- Very Low Profile Dual in-line memory module(VLP-DIMM)
- Power supply: VDD= 1.5V + 0.075V
- Interface: SSTL_15
- Programmable CAS Latency(CL): 6,7,8 support
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- DM masks write data-in at the both rising and falling edges of the data strobe
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Refresh: Auto-Refresh, Self-Refresh
- On Die Thermal Sensor supported(JEDEC optional)
- 8 bit pre-fetch
- Lead-Free Products are RoHS compliant
- Average Refresh Period 7.8us at 0℃ ≦TC≦85℃
  3.9us at 85℃ ≦TC≦95℃

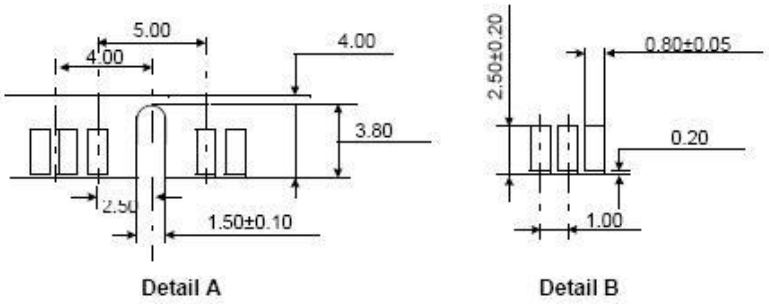
Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support			CL-tRCD-tRP
		CL6	CL7	CL8	
DDR3-1066	PC3-8500	800	1066	1066	7-7-7

Package Dimensions

Unit: mm





Tolerances : ± 0.15mm unless otherwise specified